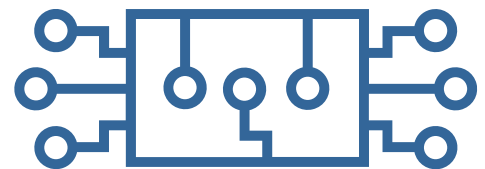

PED-Board V5

User Manual r1.0



PED-Board
just add power

1. Limited Warranty

This document is provided 'as is' and is subject to being changed, without notice, in future editions. For the latest version, refer to www.ped-board.com.

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Do not use in life support and medical applications. In such cases email to support@ped-board.com

Use the PED-Board V5 with its dedicated LabVIEW CLIP. CLIPs from previous PED-board release (V4, V3, V2 and V1) are not compatible and may damage the PED-Board V5.



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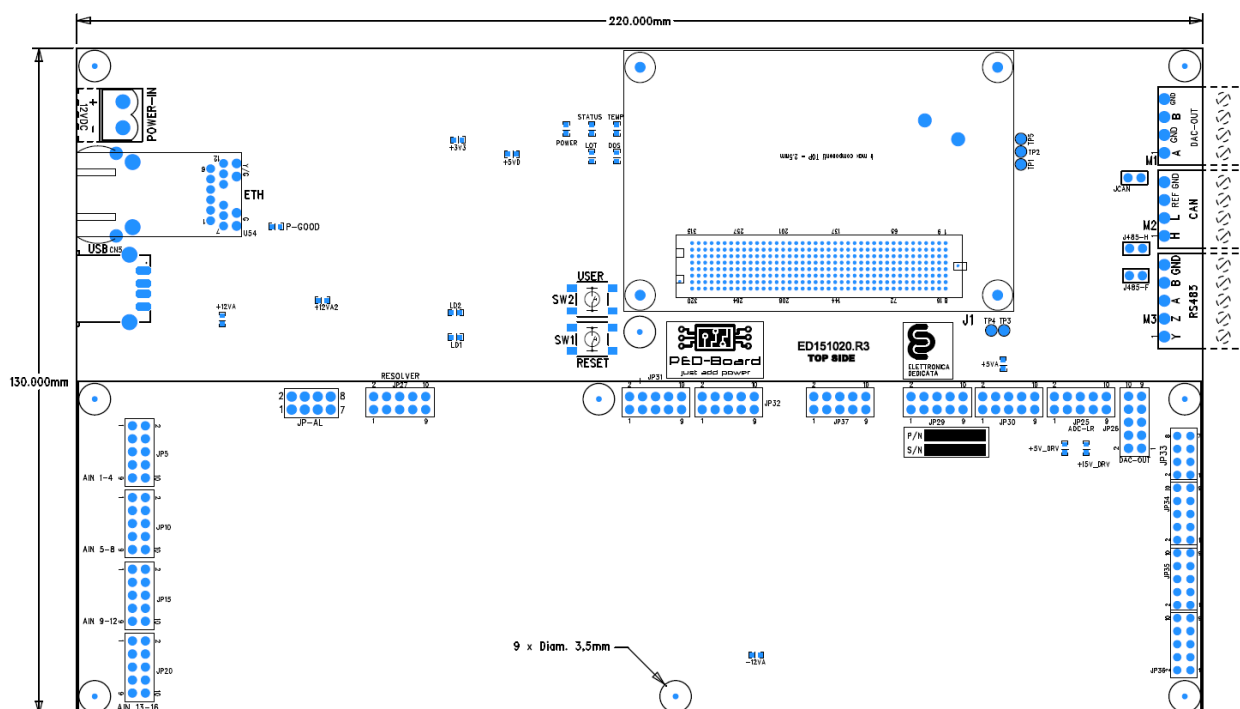


2. Electrical Specifications

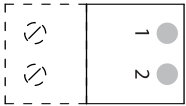
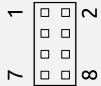
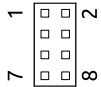
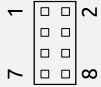
Input voltage supply (V_{in})*	+12V \pm 10% (No reverse voltage protection)
Input current	2,5A (maximum current at V_{in})
Storage temperature (IEC 60068-2-1, IEC 60068-2-2)	-40 to 85 °C
Operating temperature	-25 to 60 °C
Operating humidity (IEC 60068-2-56)	10 to 90% RH, noncondensing
Storage humidity (IEC 60068-2-56)	5 to 95% RH, noncondensing
Maximum altitude	5000 m
Pollution Degree (IEC 60664)	2
Analog inputs AINx (ADC1, ADC2) max voltage	\pm 11V
Analog inputs AINx (ADC3) max voltage	+5.1V

*Do not apply an input voltage higher than 14V at the V_{in} terminal with respect to GND





3. Layout



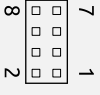
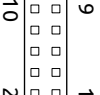
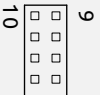
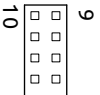
4. Connections

Connector	Pin	Name	Range	Description
CN-12V  2P P5.08mm male	1	+12V		<i>OMNIMATE SL, Weidmüller – RS Code: 403-998, compatible mating connector is available in Farnell under Code: 1729275.</i>
	2	GND		
JP-AL  2x4 Header P2.54mm	1	AGND		Filtered analog ground, derived after the internal EMI filter. Serves as the reference ground for the entire board's circuitry
	2	+5V		Regulated supply referenced to AGND. Provides up to 100 mA.
	3	AGND		Filtered analog ground, derived after the internal EMI filter. Serves as the reference ground for the entire board's circuitry
	4	+12V		Regulated supply referenced to AGND. Provides up to 100 mA.
	5	AGND		Filtered analog ground, derived after the internal EMI filter. Serves as the reference ground for the entire board's circuitry
	6	-12V		Regulated supply referenced to AGND. Provides up to 100 mA
	7	GND		Direct ground connection from the main power input
	8	+12V (Vout)		Unregulated output referenced to GND, directly connected to the main +12 V input supply. Supports up to 350 mA.
JP5  2x4 Header P2.54mm	1	AIN-1P	-5 V ↔ +5 V	Input range selection through JP6
	2	AIN-1N		
	3	AIN-2P		Input range selection through JP38
	4	AIN-2N		
	5	AIN-3P		Input range selection through JP39
	6	AIN-3N		
	7	AIN-4P		Input range selection through JP40
	8	AIN-4N		
JP10  2x4 Header P2.54mm	1	AIN-5P	-5 V ↔ +5 V	Input range selection through JP41
	2	AIN-5N		
	3	AIN-6P	Input range selection through JP42	
	4	AIN-6N		
	5	AIN-7P	0 V ↔ +10 V	Input range selection through JP43
	6	AIN-7N		
	7	AIN-8P		Input range selection through JP44
	8	AIN-8N		

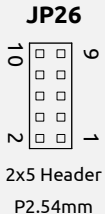
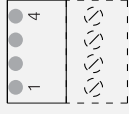
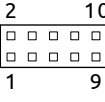

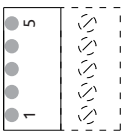



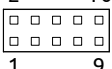

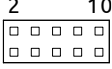
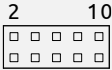
Connector	Pin	Name	Range	Description	
<p>JP15</p>  <p>2x4 Header P2.54mm</p>	1	AIN-9P	-5 V ↔ +5 V	Input range selection through JP45	
	2	AIN-9N			
	3	AIN-10P		Input range selection through JP46	
	4	AIN-10N			
	5	AIN-11P		Input range selection through JP47	
	6	AIN-11N			
	7	AIN-12P		Input range selection through JP48	
	8	AIN-12N			
<p>JP20</p>  <p>2x4 Header P2.54mm</p>	1	AIN-13P	-5 V ↔ +5 V	Input range selection through JP49	
	2	AIN-13N			
	3	AIN-14P		Input range selection through JP50 to	
	4	AIN-14N			
	<p>JP25</p>  <p>2x5 Header P2.54mm</p>	5	AIN-15P	0 V ↔ +10 V	Input range selection through JP51
		6	AIN-15N		
		7	AIN-16P		Input range selection through JP52
		8	AIN-16N		
<p>JP25</p>  <p>2x5 Header P2.54mm</p>	1	AIN-17	0 V ↔ +5 V		
	2	AIN-18			
	3	AIN-19			
	4	AIN-20			
	5	AIN-21			
	6	AIN-22			
	7	AIN-23			
	8	AIN-24			
	9	AGND			
	10				



Connector	Pin	Name	Range	Description
<p>JP33</p>  <p>2x4 Header P2.54mm</p>	8	PWM-10	0 V → +5 V	Output range selection through JP2
	7	PWM-9		
	6	PWM-8		
	5	PWM-7		
	4	PWM-6		
	3	PWM-5		
	2	DGND		
	1			
<p>JP34</p>  <p>2x5 Header P2.54mm</p>	10	PWM-4	0 V → +5 V	Output range selection through JP3
	9	PWM-3		
	8	PWM-2		
	7	PWM-1		
	6	PWM-20		
	5	PWM-19		
	4	PWM-18		
	3	PWM-17		
	2	DGND		
	1			
<p>JP35</p>  <p>2x5 Header P2.54mm</p>	10	PWM-16	0 V → +5 V	Output range selection through JP3
	9	PWM-15		
	8	PWM-14		
	7	PWM-13		
	6	PWM-12		
	5	PWM-11		
	4	PWM-30		
	3	PWM-29		
	2	DGND		
	1			
<p>JP36</p>  <p>2x5 Header P2.54mm</p>	10	PWM-28	0 V → +15 V	Output range selection through JP4
	9	PWM-27		
	8	PWM-26		
	7	PWM-25		
	6	PWM-24		
	5	PWM-23		
	4	PWM-22		
	3	PWM-21		
	2	DGND		
	1			

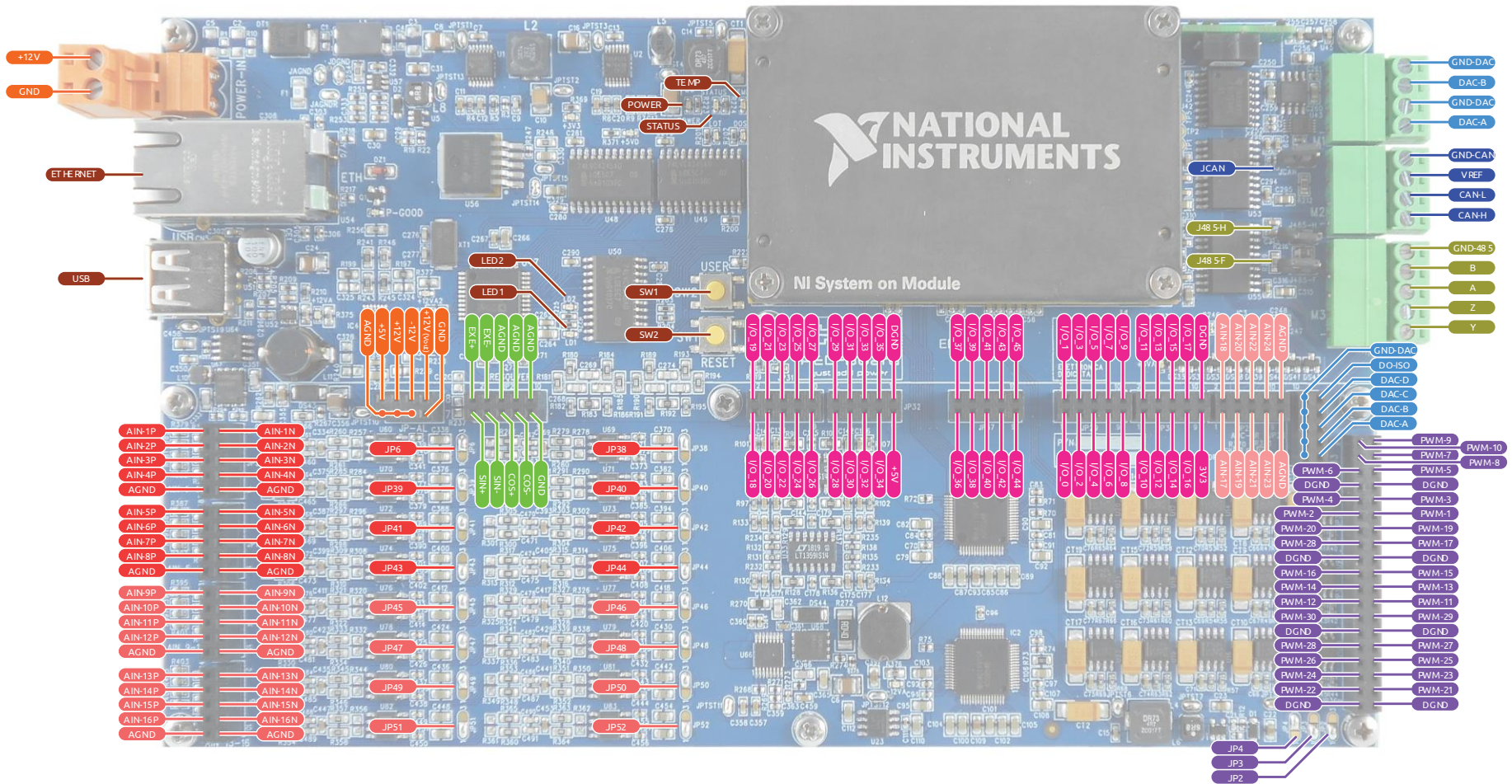


Connector	Pin	Name	Range	Description	
 <p>JP26 2x5 Header P2.54mm</p>	1	DAC-A	0 V → +5 V	1	 <p>M1 <i>Fast DAC connector</i></p>
	2	GND-DAC		2	
	3	DAC-B		3	
	4	GND-DAC		4	
	5	DAC-C			
	6	GND-DAC			
	7	DAC-D			
	8	GND-DAC			
	9	DO-ISO			
	10	GND-DAC			
 <p>JP27 2x5 Header P2.54mm</p>	1	SIN+			
	2	EXE+			
	3	SIN-			
	4	COS+			
	5	AGND			
	6	COS-			
	7	AGND			
	8	AGND			
	9	AGND			
	10	AGND			
 <p>M2 <i>Fast CAN connector</i></p>	1	CAN-H		120 Ω termination resistor can be inserted if needed, by closing the jumper JCAN	
	2	CAN-L			
	3	VREF			
	4	GND-CAN			
 <p>M3 <i>Fast RS-485 connector</i></p>	1	Y		Both the TX and RX channels are equipped with their own 120 Ω termination resistors, which can be enabled by closing the jumpers J485-F (for TX) and J485-H (for RX).	
	2	Z			
	3	A			
	4	B			
	5	GND-RS485			

Connector	Pin	Name	Range	Description
<p>JP29</p> <p>2 10</p>  <p>1 9</p> <p>2x5 Header P2.54mm</p>	1	I/O_0	0 V ↔ +3.3 V	
	2	I/O_1		
	3	I/O_2		
	4	I/O_3		
	5	I/O_4		
	6	I/O_5		
	7	I/O_6		
	8	I/O_7		
	9	I/O_8		
	10	I/O_9		
<p>JP30</p> <p>2 10</p>  <p>1 9</p> <p>2x5 Header P2.54mm</p>	1	I/O_10		
	2	I/O_11		
	3	I/O_12		
	4	I/O_13		
	5	I/O_14		
	6	I/O_15		
	7	I/O_16		
	8	I/O_17		
	9	3.3V		
	10	DGND		
<p>JP31</p> <p>2 10</p>  <p>1 9</p> <p>2x5 Header P2.54mm</p>	1	I/O_18		
	2	I/O_18		
	3	I/O_20		
	4	I/O_21		
	5	I/O_22		
	6	I/O_23		
	7	I/O_24		
	8	I/O_25		
	9	I/O_26		
	10	I/O_27		
<p>JP32</p> <p>2 10</p>  <p>1 9</p> <p>2x5 Header P2.54mm</p>	1	I/O_28		
	2	I/O_29		
	3	I/O_30		
	4	I/O_31		
	5	I/O_32		
	6	I/O_33		
	7	I/O_34		
	8	I/O_35		
	9	+5V		
	10	DGND		
<p>JP37</p> <p>2 10</p>  <p>1 9</p> <p>2x5 Header P2.54mm</p>	1	I/O_36		
	2	I/O_37		
	3	I/O_38		
	4	I/O_39		
	5	I/O_40		
	6	I/O_41		
	7	I/O_42		
	8	I/O_43		
	9	I/O_44		
	10	I/O_45		



5. Mapping on the board



6. System Architecture and Peripheral Modules

This section provides an overview of the PED-Board’s hardware architecture, and the peripheral modules integrated around the National Instruments sbRIO-9651 System on Module (SoM). The diagram below in Figure 1 illustrates the main functional blocks and communication interfaces of the board.

Each module connected to the sbRIO-9651 plays a distinct role in enabling real-time control, signal acquisition, and communication with external systems. The following subsections detail the function and specifications of each peripheral.

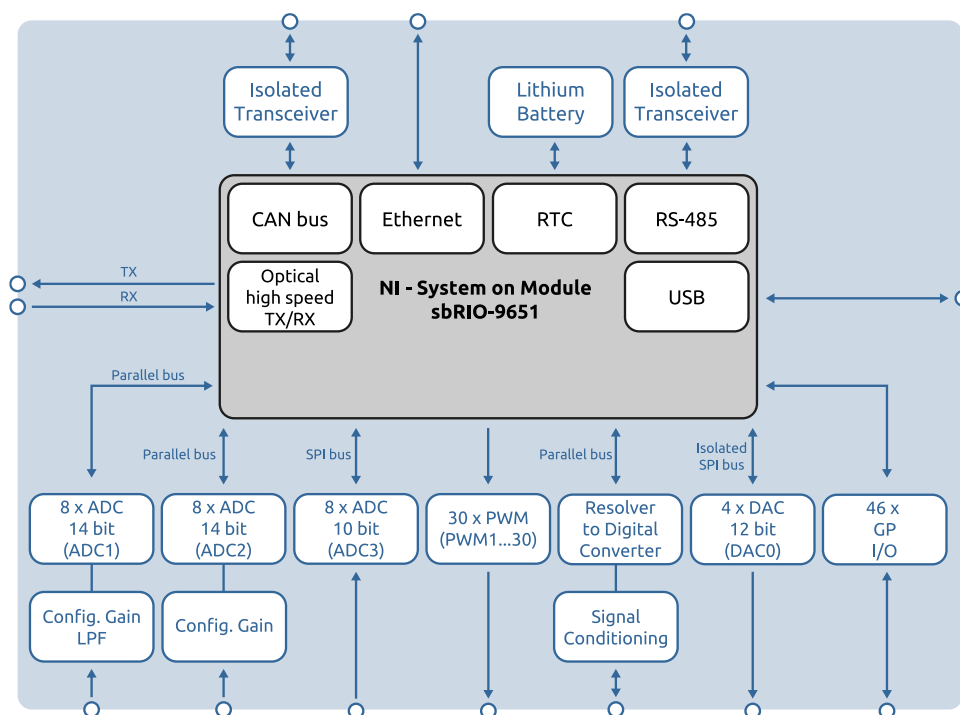


Figure 1 - Block diagram of the PED-Board system architecture

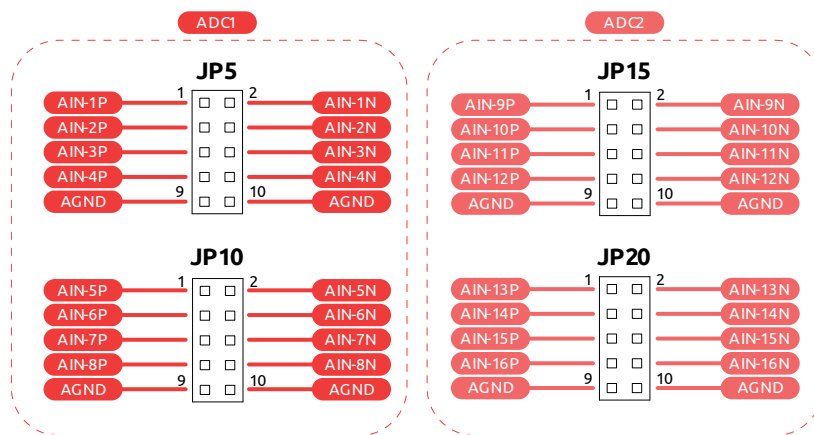


6.1. Analog-to-Digital (ADC) converters

The PED-Board features three independent ADCs blocks, labeled **ADC1**, **ADC2**, and **ADC3**.

- **ADC1** and **ADC2** are each equipped with dedicated scaling and filtering (only for ADC1) circuits, designed to condition analog signals before conversion. A detailed explanation of these front-end circuits is provided in the sections below.
- **ADC3** offers raw analog inputs without any integrated signal conditioning, giving the user full flexibility to connect application-specific sources such as temperature sensors or other analog signals requiring custom interfacing.

6.1.1. ADC1 and ADC2



ADC1 and ADC2 each provide 8 channels with simultaneous sampling capability and a resolution of 14 bits. The complete sampling and conversion process for all channels takes approximately 1.45 μs, enabling a maximum throughput of 600 kS/s.

The channels of ADC1 are mapped into inputs AIN1 to AIN8 with their respective P (positive) and N (negative) terminals accessible through connectors **JP5** and **JP10**.

The channels of ADC2 are mapped into inputs AIN9 to AIN16 with their respective P (positive) and N (negative) terminals accessible through connectors **JP15** and **JP20**.

Each channel is followed by a configurable analog front-end, supporting both bipolar and unipolar inputs. Signal scaling is achieved by adjusting a resistor value in the input stage. Filtering is handled by a second-order Butterworth active filter with a fixed gain of 1 only for the channels of ADC1. A simplified block diagram of the ADC1 and ADC2 acquisition chain is shown in Figure 2.



Figure 2 - ADC1 and ADC2 measurement chain

The ADC1 and ADC2 are designed to always digitize voltages in the range of -5 V to +5 V at its internal input pins. To accommodate wider signal ranges, a level shifting circuit is available (through a jumper selection) on each channel:



- For **bipolar** signals (± 5 V): The input is directly passed. A signal of 0 V maps to 0 V at the ADC input.
- For **unipolar** signals (0 V to +10 V): A **-5 V offset** is applied by the level shifting circuit, mapping the input range to the ADC’s native -5 V to +5 V range. In this configuration, 0 V at the input becomes -5 V at the ADC, and +10 V becomes +5 V.

Warning: The absolute maximum input voltage on each ADC1 and ADC2 pin is ± 11 V. Exceeding this limit may damage the board.

The scaling gain of the input stage denoted as G_{sc} is defined as:

$$G_{sc} = 1 + \frac{49.4k\Omega}{R_g} \tag{1}$$

By default, R_g is **not mounted**, resulting in a gain of 1. This means the maximum full-scale input voltage at the ADC1 and ADC2 connectors is: ± 5 V in bipolar mode and 0 V to +10 V in unipolar mode.

All ADC1 and ADC2 inputs are fully differential and should be connected between the P (positive) and N (negative) terminals. The converter processes the voltage difference (P – N). The level shifting circuit can be enabled per channel to support either unipolar or bipolar input ranges. Input mode selection is managed via jumpers:

- Pin 2 shorted to Pin 1 (2-1): unipolar mode
- Pin 2 shorted to Pin 3 (2-3): bipolar mode

The default configuration for the channels of ADC1 and ADC2 and respective R_g designators for the scaling gain are shown in Table I.

Table I – ADC1 and ADC2 default configuration and R_g designators

	Channel	R_g	Jumper	Jumper default
ADC1	AIN-1	R257	JP6	(2-3) Bipolar -5V → 5 V
	AIN-2	R278	JP38	
	AIN-3	R284	JP39	
	AIN-4	R290	JP40	
	AIN-5	R296	JP41	
	AIN-6	R302	JP42	
	AIN-7	R308	JP43	(2-1) Unipolar 0 V → +10 V
	AIN-8	R314	JP44	
ADC2	AIN-9	R320	JP45	(2-3) Bipolar -5V → 5 V
	AIN-10	R326	JP46	
	AIN-11	R332	JP47	
	AIN-12	R338	JP48	
	AIN-13	R344	JP49	
	AIN-14	R350	JP50	
	AIN-15	R356	JP51	(2-1) Unipolar 0 V → +10 V
	AIN-16	R362	JP52	



The filtering stage of ADC1 is implemented using a second-order low-pass Butterworth active filter based on a multiple-feedback topology, as shown in Figure 6.

By default, the PED-Board is shipped with the filter cut-off frequency set to 20 kHz (*custom filter configuration available for orders of 5 or more units*).

The filter is built around the LT1359CS14 operational amplifier from Linear Technologies. For more detailed electrical characteristics and limitations, users are encouraged to consult the corresponding datasheet.

If a different cut-off frequency is required, the filter can be modified by replacing specific passive components on the board. The correspondence between the general schematic elements (such as resistors and capacitors) and their actual designators on the PED-Board PCB is provided in Table II.

Warning: Replacing these components involves working with surface-mount parts, and appropriate care must be taken during the soldering process to avoid damaging the board.

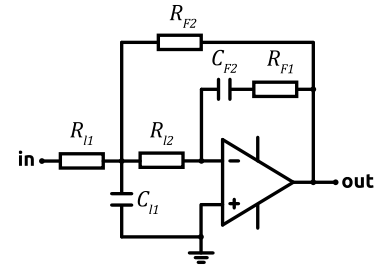


Figure 3 – Electrical scheme of the II order Butterworth filter

Table II – Board designators for the filter components

ADC1 channel	R_{11}	R_{12}	C_{11}	R_{F1}	R_{F2}	C_{F2}
AIN-1	R_{97}	R_{99}	C_{139}	Do not change	R_{228}	C_{137}
AIN-2	R_{102}	R_{103}	C_{143}		R_{229}	C_{141}
AIN-3	R_{107}	R_{106}	C_{146}		R_{231}	C_{142}
AIN-4	R_{101}	R_{100}	C_{140}		R_{230}	C_{138}
AIN-5	R_{130}	R_{131}	C_{173}		R_{232}	C_{171}
AIN-6	R_{134}	R_{135}	C_{177}		R_{233}	C_{175}
AIN-7	R_{139}	R_{138}	C_{180}		R_{235}	C_{176}
AIN-8	R_{133}	R_{132}	C_{174}		R_{234}	C_{172}

Inside the LabVIEW FPGA, the `ADC1_Read.vi` and `ADC2_Read.vi` subVIs output a 14-bit signed value in two’s complement format, regardless of input type:

In **bipolar** mode, the output directly corresponds to the input range:

- -5 V → -8192
- 0 V → 0
- +5 V → +8191

In **unipolar** mode, due to the -5 V offset:

- 0 V (input) → -8192 (ADC reads as -5 V)
- +10 V (input) → +8191 (ADC reads as +5 V)

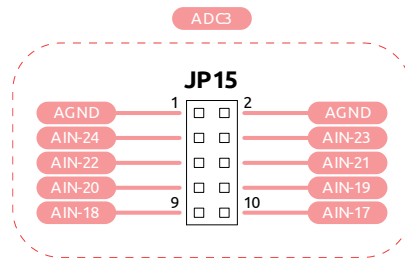
In this case, digital compensation is required to obtain the correct unipolar value. To recover the original 0–10 V range, add 8192 to the ADC output:

$$\text{Unipolar Output} = \text{ADC Output} + 8192$$

This ensures the digital range maps linearly from 0 to 16383.



6.1.2. ADC3

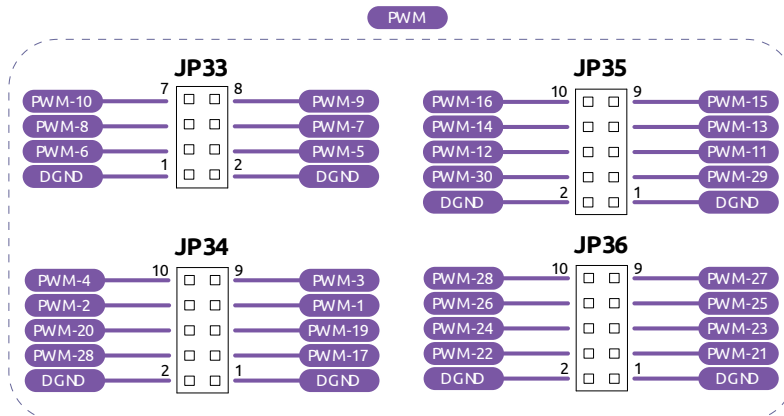


The ADC3 analog interface provides 8 single-ended input channels with 10 bits resolution data acquisition with a sampling rate of up to 200 kS/s. Communication between ADC3 and the NI sbRIO-9651 is handled via an SPI bus. The input signals AIN17 to AIN24 are accessible through connector **JP25**.

The supported input voltage range is unipolar, from 0 V to +5 V, corresponding to an output digital code ranging from 0 to $2^{10}-1$ (i.e., 0 to 1023). No signal conditioning, filtering, or scaling circuitry is provided for ADC3 inputs, so external analog processing must be implemented by the user if required.

Unlike ADC1 and ADC2, the channels of ADC3 do not support simultaneous sampling. Instead, each input must be read sequentially using the dedicated subVI [ADC3_Read.vi](#).

6.2. PWM channels



The PED-Board provides 30 independent ready-to-use PWM channels, accessible through connectors **JP33**, **JP34**, **JP35**, and **JP36**.

The PWM outputs are organized in three groups of 10 channels each, and every group can be individually configured to operate with either a 0 V → 5 V or 0 V → 15 V voltage swing. When operating in the 0 V → 5 V mode, the PWM outputs can directly drive the input of standard opto-coupled gate drivers such as the ACPL-333J or HCPL-316.

Voltage swing selection is managed through configuration jumpers **JP2**, **JP3**, and **JP4**, each corresponding to a group of 10 PWM outputs. Connecting pin 2 to pin 1 on a jumper selects the 0 V → 5 V mode, powered from the on-board +5 V supply, providing up to 15 mA continuous current per output. Connecting pin 2 to pin 3 enables the 0 V → 15 V mode, which supports up to 5 mA continuous current per channel. The default connections are summarized in Table III.



Table III – PWMs default configurations

PWMs	Jumper	Jumper default
PWM1 – 10	JP2	(2-1) 0 V → +5 V
PWM11 – 20	JP3	(2-1) 0 V → +5 V
PWM21 – 30	JP4	(2-3) 0 V → +15 V

Custom PWM voltage configuration is available for orders of 5 or more units.

All PWM outputs are driven by non-inverting buffer circuits, ensuring consistent logic polarity between the control signal and the output.

If additional PWM outputs are required beyond the 30 provided on the main connectors, they can be implemented using the Digital I/O pins of the NI sbRIO-9651. In this case, the voltage level and current driving circuits must be implemented directly on the application-specific Adapter Board, according to the needs of the final system.

6.3. Digital-to-Analog (DAC) converter

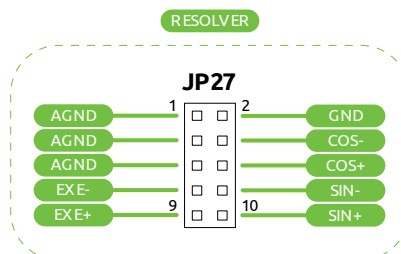


The digital-to-analog interface on the PED-Board is implemented using a fast, low settling-time DAC with an SPI communication interface. The output voltage ranges from 0 V to +5 V and is galvanically isolated from the board ground, allowing direct connection to external analog circuits without introducing ground loops or noise coupling.

The DAC has a 12-bit resolution, providing digital output values from 0 to 4095, with the full-scale output corresponding to +5 V. All DAC outputs share a common isolated ground, which is also used by an additional isolated digital output channel (DO-ISO) available on the same connector.

For applications requiring faster access to DAC outputs an additional streamlined connector (**M1**) is provided. This enables fast integration in systems.

6.4. Resolver



The resolver interface is primarily based on the Analog Devices AD2S1205YST integrated circuit. The excitation signal is generated as a differential output, buffered by an on-board current amplifier to ensure proper driving capability. The Sin/Cos acquisition circuits are designed to support various types of resolvers and include a scaling stage that can be easily configured by replacing specific resistors to match different signal levels.



The amplitude of the carrier excitation signal is adjustable, with a maximum peak voltage of 10 V, allowing compatibility with a wide range of resolver types. The excitation driver can directly supply both rotary transformer-based resolvers and switched reluctance architectures. The schematic of the excitation circuit is shown in Figure 4 with further details provided in [1]. Both excitation lines (EXE+ and EXE-) share the same amplification circuit topology.

Detailed guidelines on how to select component values for the excitation stage are also available in [1]. The Sin/Cos signal acquisition circuit is illustrated in Figure 5, where each input signal includes three configurable resistors to properly scale the resolver feedback signals. Specifically, for the Sin channel, the relevant resistors on the PED-Board are **R182** (R_{s1}), **R183** (R_{s2}), and **R186** (R_{s3}), while for the Cos channel, they are **R191** (R_{s1}), **R192** (R_{s2}), and **R195** (R_{s3}).

Default resistor values and additional configuration details are provided in Table IV. If a resistor is marked as "not mounted," it indicates that the component is intentionally left unpopulated for configuration flexibility. The resolver interface signals, including excitation and feedback lines, are accessible through connector **JP27**.

Custom resolver configuration is available for orders of 5 or more units.

Table IV - Resolver circuit components

	EXE+	EXE-		Sin	Cos
R_{e1}	R197 (24 k Ω)	R199 (24 k Ω)	R_{s1}	R182 (5.6 k Ω)	R191 (5.6 k Ω)
R_{e2}	R236 (15 k Ω)	R238 (15 k Ω)	R_{s2}	R183 (12 k Ω)	R192 (12 k Ω)
R_{b1}	R241 (12 k Ω)		R_{s3}	R186 (5.6 k Ω)	R195 (5.6 k Ω)
R_{b2}	R243 (27 k Ω)				
C_{e1}	C324	C325			
R_{f1}	R239	R240			
C_{f1}	C327	C328			
R_{fo}	R237				
C_{fo}	C326				

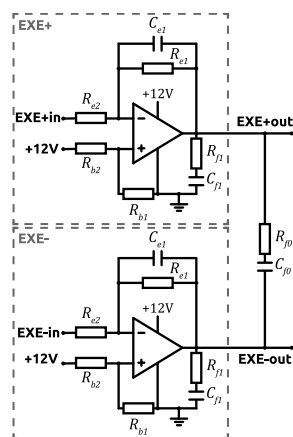


Figure 4 - Electrical scheme of the resolver excitation circuit

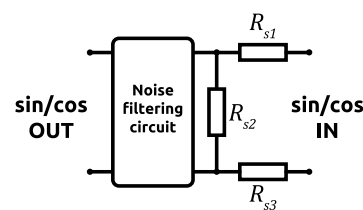
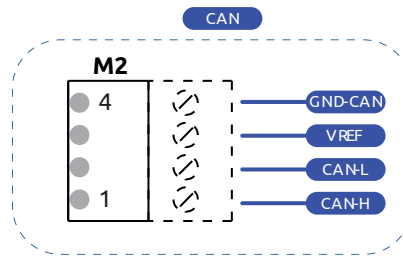


Figure 5 - Resolver Sin/Cos scaling and acquiring circuit

6.5. CAN-bus



The PED-Board includes an isolated CAN transceiver capable of supporting data rates of up to 1 Mbit/s. The CAN communication protocol can be implemented directly on the FPGA using a LabVIEW CLIP (Component-Level IP), allowing for flexible integration of the CAN controller as needed.

Implementing the CAN controller in FPGA logic requires a portion of the available resources. On average, the estimated utilization is approximately 5.9% of Slice Registers, 12.5% of Slice LUTs, and 10% of Block RAMs, with no consumption of DSP48 resources. This relatively low resource usage enables efficient integration within complex control architectures without significant impact on overall FPGA capacity.

The physical CAN interface is accessible via the dedicated connector (**M2**), which provides the isolated CAN communication lines ready for direct connection to external CAN networks.

When CAN communication is not required, FPGA resources can be optimized by simply removing the CAN controller from the generated CLIP. This allows the available FPGA space to be fully allocated to other tasks within the application.

To generate the CLIP with CAN functionality enabled, it is necessary to specify the sbRIO-9651 FPGA pins assigned to the CAN transmit (TX) and receive (RX) lines. The PED-Board’s CAN is internally connected to the sbRIO-9651 and can be accessed inside LabVIEW with the variables *CAN_TX* and *CAN_RX* within the default supplied CLIP.

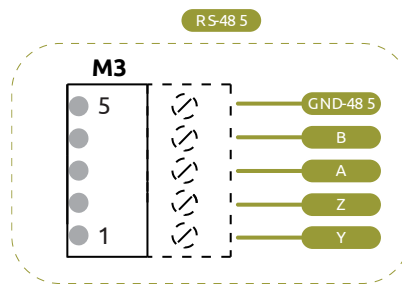
R213 is used to set up the slope of the CAN-bus data (default 0Ω). 120 Ω termination resistor can be inserted if needed, by closing the jumper **JCAN**.

6.5.1. Second CAN controller

A second CAN-bus controller can be implemented by the LabVIEW CLIP generator, and it will be available to the Digital I/O pins. The required transceiver must be placed directly on the Adapted Board.



6.6. RS-485



An RS-485 communication port can be implemented on the PED-Board using the LabVIEW CLIP Generator. The board is equipped with an isolated RS-485 transceiver, accessible through the dedicated connector **M3**.

The default CLIP defines the variables of Table V, which defines the routing of the transmit (TX) and receive (RX) signals.

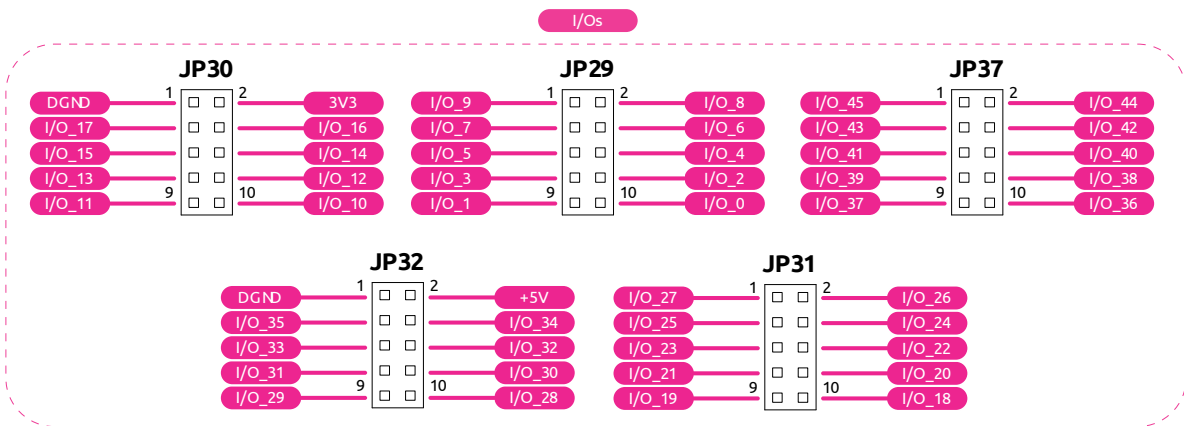
Table V - Pin routing between the RS-485 transceiver and the sbRIO-9651

PED-Board CLIP	Description
RS485_TX_EN	Transceiver TX enable pin
RS485_TX	Transceiver TX pin
RS485_RX	Transceiver RX pin
RS485_RX_EN	Transceiver RX enable pin

Both the TX and RX channels are equipped with their own 120 Ω termination resistors, which can be enabled by closing the jumpers J485-F (for TX) and J485-H (for RX). When operating in half-duplex mode, only one termination resistor should be enabled to correctly match the bus impedance and avoid signal reflections.



6.7. Digital I/O



Additional digital I/O pins are accessible via connectors **JP29**, **JP30**, **JP31**, **JP32**, and **JP37**, which enable direct routing of FPGA signals to the Adapter Board.

These digital I/O lines are directly connected to the ZYNQ-7020 FPGA pins on the sbRIO-9651. Users should refer to the Xilinx ZYNQ-7020 datasheet for detailed electrical specifications, including voltage levels, current limitations, and protection guidelines.

The PED-Board includes a dedicated digital interface for the direct connection of low-resolution Hall-effect position sensors, without requiring additional interface circuitry. These sensors can be connected to the Digital I/O ports **JP29**, **JP30**, **JP31**, **JP32**, and **JP37**. In addition to the I/O signals, the connectors provide non-isolated auxiliary power supplies of +3.3 V and +5 V, which can be used to directly power Hall-effect sensors, encoders, or other low-power digital devices. Each auxiliary supply offers a maximum output current of 100 mA per rail, enabling straightforward sensor integration into the control system.



6.8. Status and User LEDs, User button and Reset, USB port

The PED-Board is equipped with three system LEDs that indicate the operating status of the sbRIO-9651 module:

- POWER (green) – Indicates that the board is powered.
- STATUS (yellow) – Provides system status information.
- TEMP (red) – Signals temperature-related warnings or faults.

For a detailed description of the behavior and meaning of these LEDs, please refer to the National Instruments sbRIO-9651 System-on-Module datasheet.

In addition to the system LEDs, the board includes two user-programmable LEDs, both green, which can be directly controlled from the FPGA accessing the variables `LED1` and `LED2`.

The sbRIO-9651 reset function can be triggered by pressing **SW1**, while **SW2** serves as a user-configurable push button, with a default state of logic low when unpressed. SW2 is connected to the FPGA and accessed with the variable `SW2`.

The onboard USB port (USB1) operates exclusively as a USB Host, allowing the connection of compatible peripherals such as memory drives or input devices.

6.9. RTC Battery

The PED-Board is equipped with a Lithium battery dedicated to powering the Real-Time Clock (RTC) of the NI System-on-Module. This ensures that date and time information are retained even when the main power supply is disconnected. The installed battery is a 3 V, 35 mAh CR-1220 Lithium coin cell, providing long-term backup for the RTC function under typical usage conditions.

6.10. Optical Link

Optical Link directly installed in the PED-Board. TX and RX pins can be accessed directly in the FPGA with the variables `TX` and `RX`.



Mate connectors

Connector	Manufacturer	Distributor
Power supply *	WEIDMULLER 1526460000	Farnell 1729275
Strip line 2x4 (JP33, JP-AL, ...)	HARWIN M20-9980446	Mouser 855-M20-9980446
Strip line 2x5 (JP27, JP34, ...)	HARWIN M20-9980546	Mouser 855-M20-9980546
CAN-bus (screw) * DAC (screw) *	On Shore Technology Inc. OSTTJ0411530	DigiKey ED10556-ND
RS-485 *	Würth Elektronik 691361100005	DigiKey 732-2754-ND

* Mate connector shipped with the control board.

7. References

- [1] Jakub Szymczak, Shane O’Meara, Johnny S. Gealon, and Christopher Nelson De La Rama, “Precision Resolver-to-Digital Converter Measures Angular Position and Velocity”, Analog Devices application note.



8. Revision History

Date	Rev #	
April 2023	1.0	
January 2025	1.1	Table 4 updated
September 2025	2.0	New Template and Review

9. Contacts

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