

PED-Board Driving 2.5 MW 3-Level NPC for Urban Railway Energy Recovery

Introduction

This project, funded by Citracc Rail, a well-known Spanish company with a long track record in the energy and railway sectors, focused on developing a control algorithm for a three-level neutral-point-clamped (NPC) converter used to feed energy from the DC catenary back into the AC grid during regenerative braking. The converter is essential for transforming the catenary's direct current into alternating current, making energy recovery possible. In general, the operation of an electric train can be divided into four phases: acceleration, cruising, coasting, and braking. During braking, the train decelerates until it stops, and the traction machine operates as a generator, converting kinetic energy into electrical energy. Unlike friction braking, this method does not produce wear, dust, heat, or noise.

In urban areas, overhead contact lines are typically supplied with DC through non-reversible conversion systems, such as diode rectifiers. Consequently, if the catenary cannot absorb the braking power, a dissipative (dynamic) braking system is activated, and the opportunity for energy recovery is lost. An advanced bidirectional railway substation is illustrated in Figure 1: during train acceleration, power flows from the grid to the catenary (condition 1). In a conventional substation, during braking, power flows from the traction system—operating as a generator—to braking resistors (condition 2), dissipating the energy as heat. In modern substations, during regenerative braking, power flows from the generator-mode traction system to the Energy Recovery System (ERS) (condition 3), which injects the power into the AC grid.

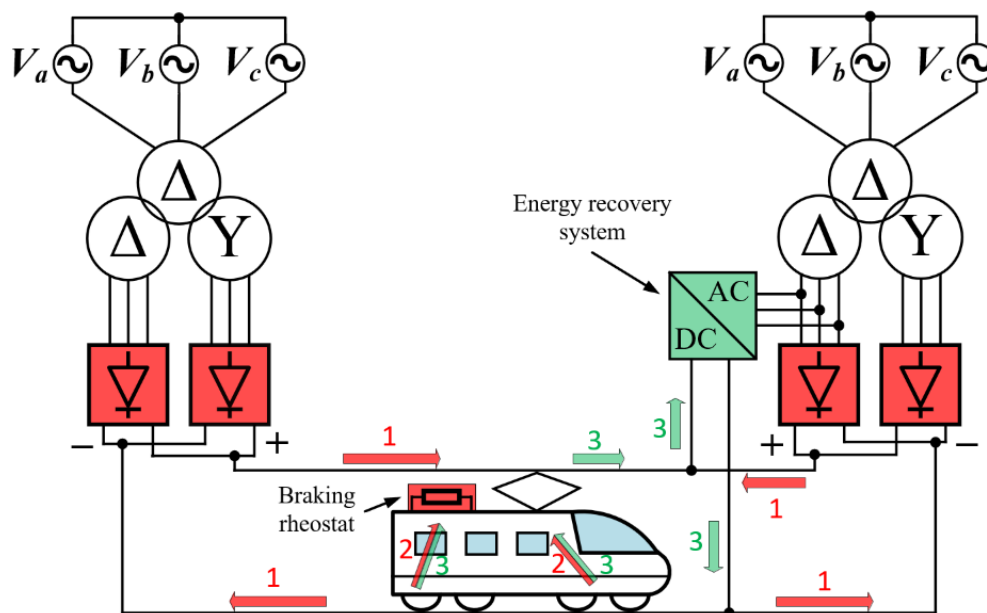


Figure 1 – Conventional and advanced train substation.

Objective

The main goal of the project is to develop a control algorithm for a 2.5-MW three-level neutral-point-clamped (NPC) converter used to feed energy from the DC catenary back into the AC grid

during train regenerative braking. This converter is essential for converting the overhead line's DC into AC, enabling energy recovery. The reference electrical schematic used to develop the control algorithm is shown in the figure.

System Description

The energy recovery system is built around several key components:

- **Three-Level NPC Converter:** This topology splits the DC-link voltage into two halves, enabling three output levels: $-V_{dc}/2$, 0 , and $+V_{dc}/2$. The result is lower harmonic content and reduced dv/dt in the output voltage and current waveforms, improving overall system efficiency.
- **PED-Board:** An advanced control platform that combines a microprocessor with an FPGA. It is programmed using LabVIEW FPGA, allowing intuitive graphical development and the integration of existing VHDL code and IP cores.
- **Dedicated Adapter Board:** A project-specific adapter that mates to the PED-Board and provides all necessary external connections, allowing the PED-Board to interface with virtually any type of power converter.

Control Strategy

As noted, the project required designing the control system for a 2.5-MW NPC converter. The challenge was to capture and feed back as much of the braking energy as possible: the window is only on the order of ten seconds, with the largest portion available at the start of braking. The algorithm therefore had to be both fast and stable. We adopted a **feed-forward** scheme combined with a **PID** controller.

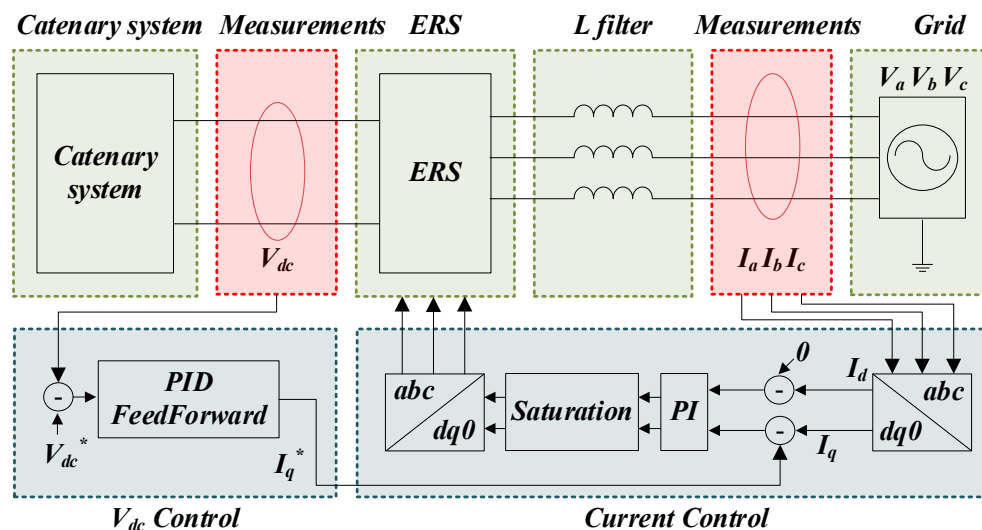


Figure 2 – Inverter control scheme.

The control is based on measuring the **catenary voltage**. During regenerative braking, injecting current into the catenary causes the voltage to rise. This rise is used as the trigger for converter

modulation. The measured voltage also serves as the reference for the algorithm's outer control loop. The block diagram of the controlled system is shown in the figure below, where **ERS** denotes the **Energy Recovery System**.

Technical Implementation

The project's technical implementation involved several stages and tools:

- **Code Partitioning (Code Splitting):** National Instruments platforms combine real-time Linux-based CPUs with FPGAs. To maximize system efficiency, tasks must be assigned to the most suitable device. This partitioning—code splitting—is essential to fully leverage the available hardware.
- **LabVIEW FPGA:** Used to program the FPGA, LabVIEW FPGA supports integrating existing VHDL code and IP cores from the Power Electronics IP Library. This lets us focus on application-specific features while reusing proven building blocks for PWM, PID control, and Clarke/Park transforms. LabVIEW also offers a customizable **Front Panel** that simplifies system interaction and makes the system's behavior easier to understand.
- **FPGA and CPU Roles:** The FPGA parallelizes and pipelines the algorithm in both time and space, while the microprocessor executes instructions sequentially. This combination provides efficient, flexible converter control. With its high execution rate and deterministic timing, the FPGA is ideal for tasks that demand precision and speed.

Below, we present how the feed-forward path and PID were implemented in LabVIEW FPGA, illustrating how graphical programming made FPGA development straightforward compared with text-based approaches.

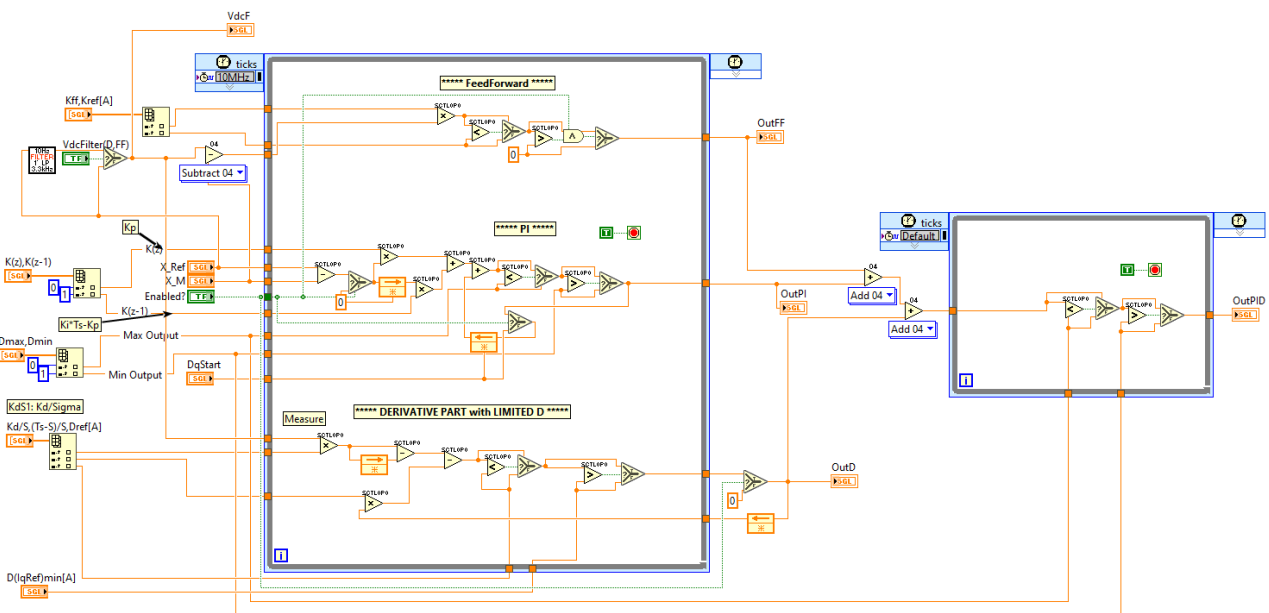


Figure 3 – Sketch of the LabVIEW FPGA control code.

Use of HIL (Hardware-in-the-Loop)

To ensure accuracy and reliability—and above all to develop and operate the control algorithm safely—we employed HIL platforms. **Hardware-in-the-Loop** is a powerful approach that lets you emulate the real physical system so the control can be tested without electrical or mechanical risk, shortening development and verification time while protecting operators. It also enables remote development and testing with reliable results and lower costs. Consequently, before deploying the algorithm on the actual system, we conducted extensive trials using the C-PED HIL platforms at Roma Tre University:

- **HIL Platforms:** Systems such as **OP4610XG** and **Typhoon HIL-606** were used to simulate and test the system in real time. These platforms make it possible to create a digital twin of the physical system, streamlining control-algorithm development and verification.
- **HIL Model:** The HIL model uses the **OPAL-RT eHS64 Gen5** solver, enabling accurate, high-fidelity simulation of the energy recovery system. This approach allowed us to test under realistic conditions, identify issues early, and resolve them prior to commissioning.

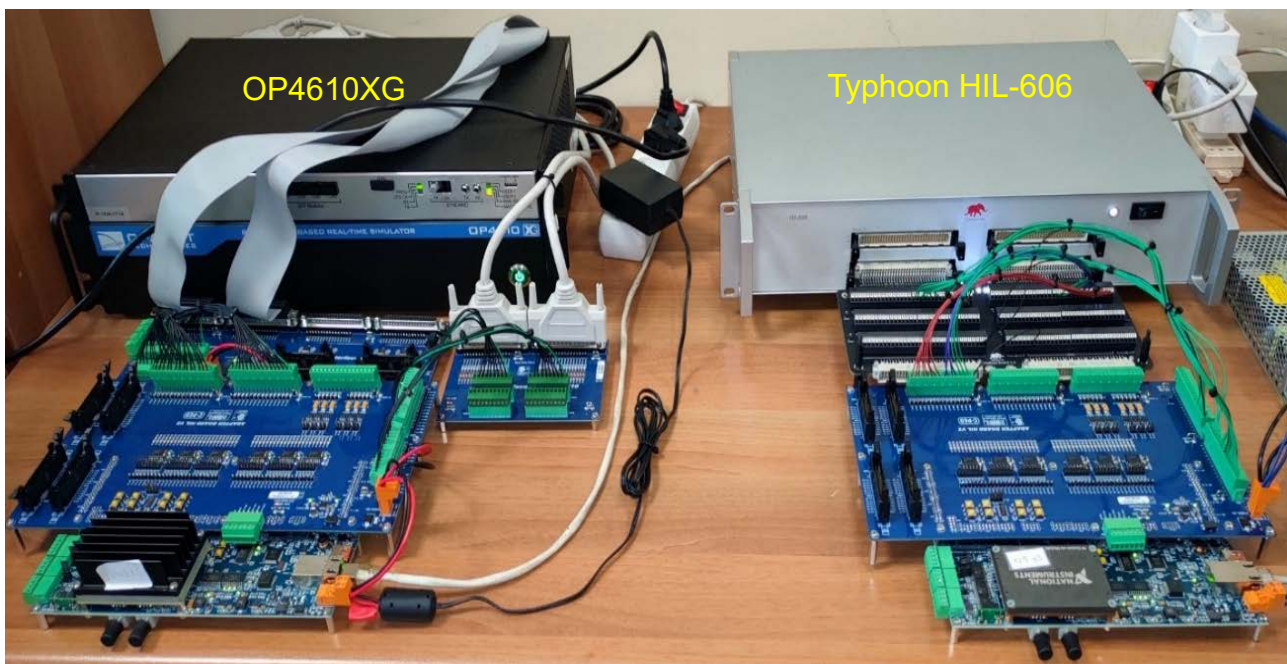


Figure 4 - HIL testbed.

PED-Board Features

The PED-Board is a crucial element of the project, with several distinctive characteristics:

- **LabVIEW RIO Architecture:** This architecture combines an FPGA and a microprocessor, offering greater flexibility and compute capability. LabVIEW FPGA's graphical programming lets you express the algorithm directly as a “block diagram,” simplifying development and maintenance.

- **IP Core Integration:** LabVIEW FPGA supports integrating existing VHDL code and IP cores from the Power Electronics IP Library, optimizing development and allowing the team to focus on application-specific features.
- **Additional I/O and Buses:** The PED-Board includes ADCs, DACs, CAN-bus, and other functions.

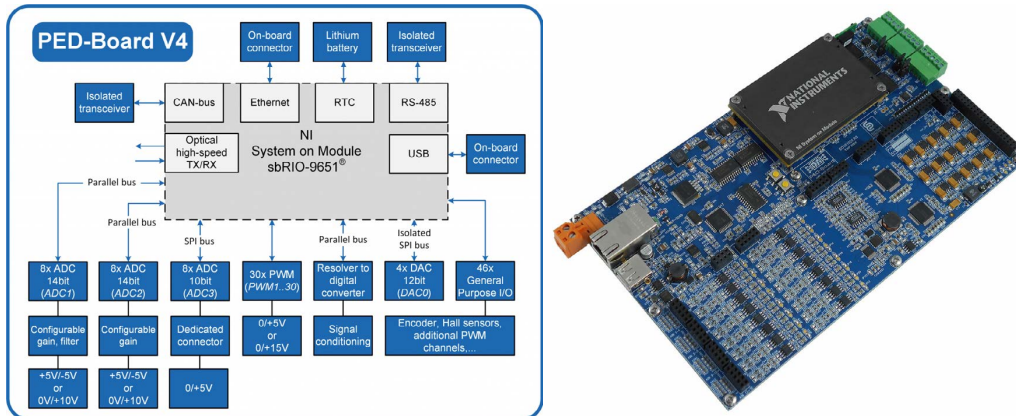


Figure 5 - PED-Board used for system deploy.

Results

The system successfully achieved its goal of recovering energy during train braking, improving the energy efficiency of electrified rail lines. The PED-Board proved effective in medium-voltage railway applications, contributing to greater sustainability and lower energy costs.

The project highlighted the central role of three-level NPC converters and the PED-Board in railway energy recovery. Combining an FPGA and a real-time processor—and programming with LabVIEW FPGA—enabled the development of a control system that is both efficient and reliable, delivering a significant improvement in the energy performance of railway infrastructure.

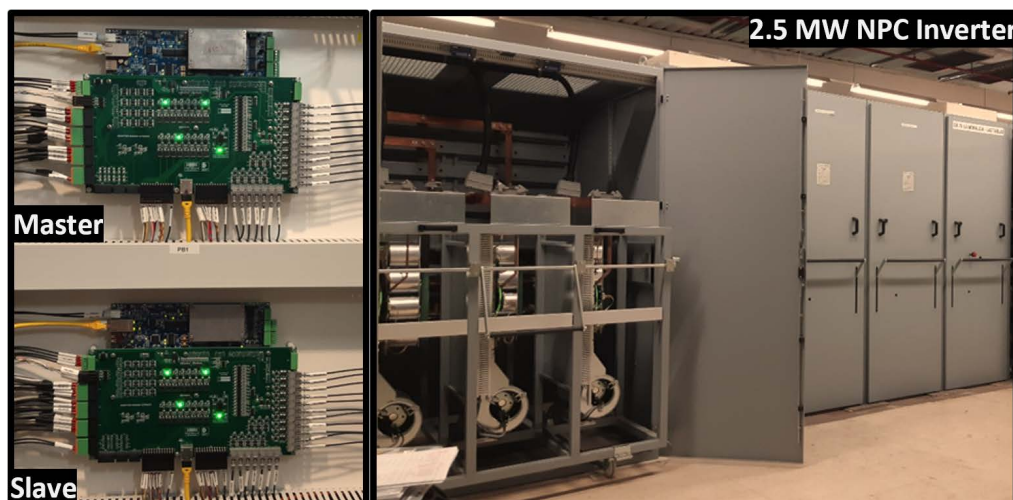


Figure 6 - Hardware realization and installation.